



Research Article

THD Minimization in Seven-Level Packed U-Cell (PUC) Inverter using Particle Swarm Optimization

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ABSTRACT

This study presents the modeling and simulation of an asymmetric seven-level Packed U-Cell (PUC) multilevel inverter employing a reduced number of power switches. A Modified Pulse Width Modulation (MPWM) scheme, optimized through the Particle Swarm Optimization (PSO) algorithm, is implemented to determine the optimal switching angles for enhanced harmonic elimination. The primary objective is to improve the output voltage waveform quality while reducing Total Harmonic Distortion (THD) and enhancing switching efficiency. The novelty of this work lies in integrating PSO with MPWM control in an asymmetric seven-level PUC inverter configuration with fewer switches, a combination that has not been previously addressed. Simulation results in Simulink demonstrate that the proposed PSO-optimized MPWM strategy achieves a THD of 17.72%, outperforming conventional modulation techniques. These findings highlight the effectiveness of intelligent optimization methods for multilevel inverter control and their potential contribution to improving power quality in renewable energy applications.



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1. INTRODUCTION

Over the past decade, the growing global demand for energy has driven a significant shift from conventional transformers to advanced power electronic systems. In particular, cost-effective switching devices are increasingly integrated into power inverters, which are essential for sustainable energy systems by enhancing efficiency and market competitiveness. Traditional two-level converters are increasingly being replaced by multilevel inverters, which operate at lower switching frequencies and offer reduced power losses and harmonic distortion [1]. Voltage source converters can be categorized based on their output waveforms into square wave, quasi-square wave, conventional two-level PWM, and multilevel inverters (MLI).

This work's innovation resides in the implementation of a 7-level PUC inverter, characterized by a diminished component count relative to conventional topologies, thereby enabling a more compact and efficient harmonic reduction system. In MLIs, switch commutation combines several DC voltages, resulting in elevated output levels at a reduced switching frequency, which mitigates losses and the stress associated with switching and voltage [2]. An inverter is an electrical device that converts DC to AC power [3]. Conventional inverters typically offer three output levels: zero, positive, and negative [4]. The PUC-MLI setup yields seven output levels utilizing eight devices, whereas the NPC, FLC, and CHB necessitate 50, 54, and 15 devices, respectively. The packed U-cell inverter, known for its U-shaped configuration, offers a broader spectrum of output voltage levels dependent on the quantity of voltage sources and switching devices employed [5]. Multilevel inverter (MLI) technology is increasingly employed in electrical systems to produce accurate waveforms with low harmonic distortion. These strategies facilitate the reduction of Total Harmonic Distortion (THD) and enhance the MLI's waveform, each offering distinct advantages related to efficiency, convergence speed, and design complexity for the optimization problem, the advantages of a more straightforward design and the capability to produce various output voltage levels render the PUC inverter a favored option for multiple applications. The maximum voltage level achievable by the PUC inverter is disadvantageously constrained. Only the peak amplitude of the inverter's DC source is applicable [6]. This study introduces a revised design for the single-

phase arrangement of Packed U-Cell inverter with seven voltage levels.

The suggested topology mimics with varied DC sources, necessitating three cells to produce an output with seven distinct voltage levels. The proposed configuration attains performance equivalent to that of the seven-level Cascaded H-Bridge inverter while utilizing fewer switches [7]. Multilevel inverters have recently garnered significant attention for their capacity to diminish overall harmonic interference and improve power quality. Among these, the PUC topology provides a higher performance with a smaller structure and fewer components. In this research, an enhanced PWM method is employed to operate a seven-level PUC inverter. To further reduce THD, the method PSO is employed to optimize the switching angles [8]. Developers have utilized population-based optimization techniques such as Genetic Algorithms (GA), Harmony Search (HS), Moth Flame Optimization (MFO), and Random Differential Algorithm (RDA) for high-level inverters [9][10]. While these approaches demonstrate effectiveness, they often involve higher computational cost and slower convergence. This study presents and utilizes the Particle Swarm Optimization method, a swarm-based optimization strategy aimed at minimizing THD in multiterminal inverters [11].

In this study, harmonic suppression was significantly enhanced through the combined effect of the compact PUC topology and the PSO-optimized MPWM scheme. By dynamically adjusting switching angles with respect to asymmetric DC voltage levels, the approach effectively attenuates low-order harmonics and improves the spectral quality of the output waveform. Prior investigations have also shown that metaheuristic techniques can achieve stronger convergence and higher accuracy in nonlinear switching problems compared to analytical methods [5]. The present work differs in its integration of PSO with MPWM, which eliminates the need for iterative lookup tables while still achieving comparable THD reduction with fewer computational resources. Improved efficiency observed in this work also corresponds with earlier studies that emphasized the importance of reduced switch counts in minimizing conduction and gate-drive losses. Unlike those investigations, which primarily focused on topological simplification, the proposed approach advances the field by combining structural reduction with optimization-based modulation. Similar ideas have been explored in recent studies that incorporated hybrid GA–PSO and other metaheuristic methods in multilevel inverters, where significant THD reductions were achieved by optimizing modulation angles while maintaining low device counts [12][13]. This dual strategy not only lowers implementation cost but also improves waveform quality, thereby enhancing inverter performance and extending applicability to renewable energy and medium-voltage drive systems. However, unlike many of those works, which achieved suppression by operating at higher switching frequencies, the proposed method demonstrates satisfactory performance even at moderate frequencies. This discrepancy may arise from differences in modulation design, parameter selection, and the use of asymmetric DC sources in the PUC structure, which provide additional flexibility for harmonic elimination. Comparable results were also noted in recent research where PSO and hybrid optimization algorithms achieved harmonic mitigation in asymmetric multilevel inverter topologies [14].

Overall, the results confirm that the PSO–MPWM framework not only reinforces the established advantages of optimization-driven control but also extends prior contributions by demonstrating that reduced-component multilevel inverter structures can simultaneously achieve superior harmonic performance, lower switching stress, and reduced implementation cost.

Despite the advantages of the PUC topology and the success of optimization algorithms in inverter control, little research has explored the integration of Particle Swarm Optimization (PSO) with a Modified PWM (MPWM) scheme in a reduced-switch seven-level PUC inverter. Prior studies have mainly applied conventional PWM techniques or optimization methods such as GA and hybrid algorithms to other inverter families like NPC and CHB, but not specifically to the asymmetric seven-level PUC. This gap is important because combining PSO with MPWM for a reduced-switch PUC can achieve lower THD while using fewer components, leading to improved efficiency, reduced switching losses, and lower implementation cost. Therefore, this study proposes a compact seven-level PUC inverter with reduced switch count and implements a PSO-optimized MPWM strategy to minimize THD. The approach is validated through Simulink simulations and compared with conventional PWM methods.

The main contributions are: a validated compact PUC topology with harmonic improvement, a reproducible PSO-based MPWM strategy tailored to the asymmetric PUC structure, and quantitative evidence of superior power quality with reduced hardware complexity.

2. RESEARCH METHODS

Multilevel inverters have drawn a lot of interest lately because of their capacity to lower total distortion factor and enhance power quality. Of these, the Packed U-Cell (PUC) topology provides a higher performance with a smaller structure and fewer components. This research employs a pulse width modulation (PWM) approach to control a seven-level PUC inverter system. To further lower THD, the adopted metaheuristic method was executed to fine-tune the switching angles. The work in (2022) [15], which also used a Grey Wolf Optimizer (GWO)-optimized Modified PWM technique to regulate a 3-level NPC converter, is compared.

One piece of power electronics that can change the direction of electricity from DC to the AC voltage range is an inverter. It is utilized throughout numerous sectors, including renewable energy generation and electric vehicles, among others, a swarm-intelligence based optimization method is proposed and implemented in this study for the mitigation of harmonics and the reduction of the THD factor in multi-terminal inverters [16]. In photovoltaic systems, inverters are crucial for converting the direct current generated by solar cells. Renewable generation is achieved using PV modules in conjunction with wind turbines, which can be integrated into the power grid or used to operate conventional household electronic devices [6][17]. This study investigates the optimization of the essential procedures required to achieve the targeted output of the injected sine waveform while minimizing overall harmonic distortion.

2.1 Seven Level Packed U Cell Inverter

In 2010, Al-Haddad invented the PUC converter and the multilayer converter, which is capable of being expanded to single-phase topologies. Figure 1 depicts a system with six semiconductor switching devices and a dual DC supply. The significant model is the number of segments relative to other topologies. A reduced quantity of switches leads to lower conduction and switching losses, minimized gate driver requirements, and decreased total system costs [18]. The output voltage levels attained and the quantity of auxiliary capacitors employed can be expressed as Equation (1).

$$N_v = 2^{N_c+2} - 1 \quad (1)$$

where N_v represents count of quantized voltage levels and N_c denotes the amount of auxiliary capacitors utilized.

Table 2 presents the quantities of devices for several inverter kinds (NPC, FLC, CHB, and PUC). Six IGBTs have been employed in the PUC architecture to attain seven levels. The six gated semiconductor devices are separated into two legs, resulting in a configuration of three switches per leg. The quantity of potential states can be expressed as Equation (2).

$$N_p = 2N^s \quad (2)$$

where N_p represents the total possible states and N_s is the quantity of switches in a single leg [19][20]. This relationship directly impacts the modulation strategy and achievable output waveform quality, as a higher number of possible states allows for finer voltage steps and reduced harmonic distortion [21].

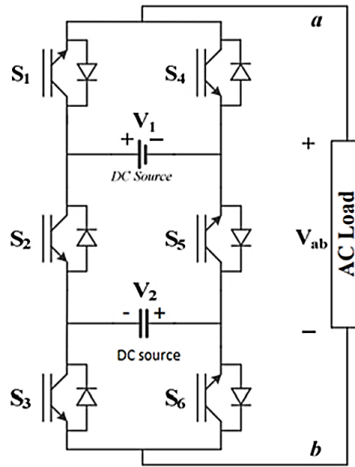


Figure 1. Structural layout of the 7-level PUC inverter

The primary advantage of PUC is its lower component count relative to other topologies, including the Cascaded H-Bridge, fewer switches lead to less power losses, fewer gate drives, and decreased overall system costs [8]. The output voltage magnitudes of the single-phase inverter configuration illustrated in Fig. 1 are listed in Table 1. There exist eight potential switching states. The upper switches in each leg function in complementarity with their respective lower switches to prevent short-circuit problems across the DC buses. Each upper-lower pair operates antagonistically to guarantee safe functioning and is unable to function simultaneously [16]. While the PUC is capable of producing different voltage levels from various DC sources, achieving the maximum output voltage (V_{ab}) necessitates that the amplitude of the second DC bus be equal to one third of the first ($V_1 = 3V_2$). V_{ab} exhibits seven voltage levels as a result of the voltage levels in this setup being $0, \pm V_2, \pm 2V_2$, and $\pm 3V_2$.

Table 1. Single-leg switching states of the PUC-MLI

| States | Voltages | S1 | S2 | S3 |
|--------|----------|----|----|----|
| 1 | V1 | 1 | 0 | 0 |
| 2 | V1 – V2 | 1 | 0 | 1 |
| 3 | V2 | 1 | 1 | 0 |
| 4 | 0 | 1 | 1 | 1 |
| 5 | 0 | 0 | 0 | 0 |
| 6 | -V1 | 0 | 0 | 1 |
| 7 | -V2 – V1 | 0 | 1 | 0 |
| 8 | -V2 | 0 | 1 | 1 |

Table 2. Device requirements for different inverter architectures

| Components | NPC | FLC | CHB | PUC |
|------------------------------|-----|-----|-----|-----|
| IGBT power devices | 24 | 24 | 12 | 6 |
| Capacitors (Voltage Sources) | 60 | 30 | 3 | 2 |
| Clamping Diodes | 20 | 0 | 0 | 0 |
| Total component | 50 | 54 | 15 | 8 |

To validate the performance of the proposed 7-level Packed U-Cell (PUC) inverter employing a PSO-based Modified Pulse Width Modulation (MPWM) strategy, a comparison is made with other PUC multilevel inverter topologies reported in recent literature. Lower-level topologies such as the 5-level PUC inverter exhibit simpler hardware and lower cost, yet they typically suffer from higher Total Harmonic Distortion (THD) due to larger voltage steps [1]. A 5-level PUC-based shunt active power filter with fuzzy control was shown to achieve effective harmonic compensation but still encountered notable residual THD [22]. A 9-level Modified PUC inverter employing a Model Predictive Control (MPC) approach demonstrated improved waveform quality and reduced THD compared to conventional 5-level designs [8]. Furthermore, an 11-level PUC inverter with an optimized eight-switch configuration for photovoltaic applications achieved additional THD reduction but required higher circuit complexity and multiple DC sources [23]. In comparison, the proposed 7-level PSO-MPWM PUC inverter provides a balanced trade-off achieving lower harmonic distortion than 5-level topologies while significantly reducing the component count and control complexity relative to higher-level designs. Therefore, the 7-level configuration represents a practical and efficient topology within the PUC inverter family, maintaining favorable output quality with fewer power devices and reduced implementation cost.

2.2 Carrier-based PWM Technique

In power electronics, especially in voltage source inverters, Carrier-Based Pulse Width Modulation (PWM) is extensively utilized across multiple applications. The power consumption of an electronic load is controlled by modifying the switching duration of the output pulses[24]. This approach maintains the carrier signal's consistent amplitude while varying the pulse lengths within the designated power level. The modulation index is defined as the ratio of pulse duration to the carrier signal period, and it governs the power supplied to the load [25]

A primary benefit of PWM is its capacity to provide a stable signal with minimal distortion. This strategy is realistic, as it reduces power dissipation in switching devices such as transistors or MOSFETs. However, its implementation may be more intricate than alternative PWM methods, requiring a distinct high-frequency carrier signal and accurate temporal regulation. Diverse carrier-based PWM schemes are available, each with unique advantages and limitations [26].

Sinusoidal pulse width modulation, in conjunction with triangular waves, minimizes overall harmonic distortion in inverters while regulating the power consumption of electrical loads. The sinusoidal pulse width modulation approach is extensively employed for the generation of pulse signals in inverter control. This study employs a reference sine wave in conjunction with multiple triangular carrier waves, utilizing six carriers to regulate six inverter switches. The total number of carriers is established according to the inverter's level setting as outlined in Equation (3).

$$N = L - 1 \quad (3)$$

Equation (3) delineates N as the number of carriers and L as the amount of voltage levels produced in the inverter architecture, employing the specific values of $L = 7$ and $N = 6$ for this examination. The construction of our topology is based on two essential principles: amplitude modulation (AM) and frequency modulation (FM). The FM index is defined as the ratio of the reference voltage signal relative to the carrier signal, normalized to unity for the sake of this study [27]. The amplitude modulation index M_a is expressed in Equation (4).

$$M_a = \frac{V_{ref}}{V_{carrier}} \quad (4)$$

$$M_f = \frac{f_{Carrier}}{f_{ref}} \quad (5)$$

This study used a 50 Hz frequency and three amplitude reference signals are used to control the inverter's output voltage according to the specified reference value. Using the modulation indices defined in Equations (4) and (5), switching pulses are produced by aligning the reference wave with carrier waves. The frequency carrier rate was established at 1000 Hz, and the modulation amplitude was set to 2 to demonstrate the significance of amplitude modulation. Figure 1 shows the MPWM technique, where a sinusoidal reference is combined with a PSO optimized injected signal. The modified reference, compared with a triangular carrier, generates PWM pulses that reduce THD.

Refer to Table 1 for details on the switch configuration and output voltage levels. When V1 is present at the output with voltage activated from S1, S5, and S6, It becomes possible to generate seven voltage levels across different modes, with S4, S5, and S6 operating as complementary switches to the first three in order to prevent short circuits. Figure 2 illustrates the gate driver output signals for the proposed seven-level PUC multilevel inverter, which is produced using a triangular carrier-based MPWM method.

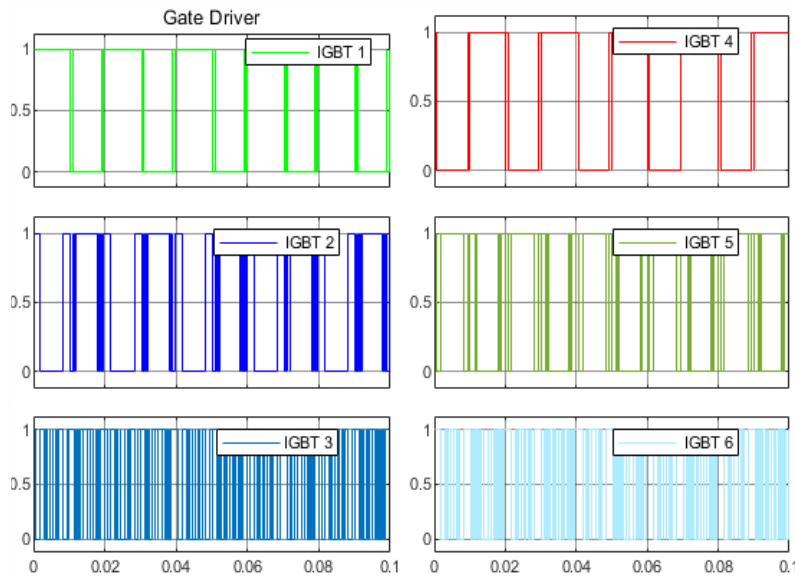


Figure 2. Switching pulse of IGBT

The MPWM methodology, illustrated in Figure 3, employs a two-signal based control comprising a sinusoidal reference signal and an optimized injected sine waveform. Optimization of parameters for the inserted signal in the MPWM methodology, encompassing magnitude, frequency, and phase characteristics, is executed via PSO. Equations (6) and (7) denote the injected and altered signals, respectively.

$$V_i(t) = a_0 \cdot \sin(2\pi f_0 t + \theta) \quad (6)$$

$$V_i(t) = 3 \cdot \sin(2\pi \cdot 50 \cdot t + 0) + a_0 \cdot \sin(2\pi f_0 t + \theta) \quad (7)$$

The optimization process conducted by PSO facilitates enhanced harmonic distortion reduction and waveform regulation, making the MPWM approach more efficacious for power electronics.

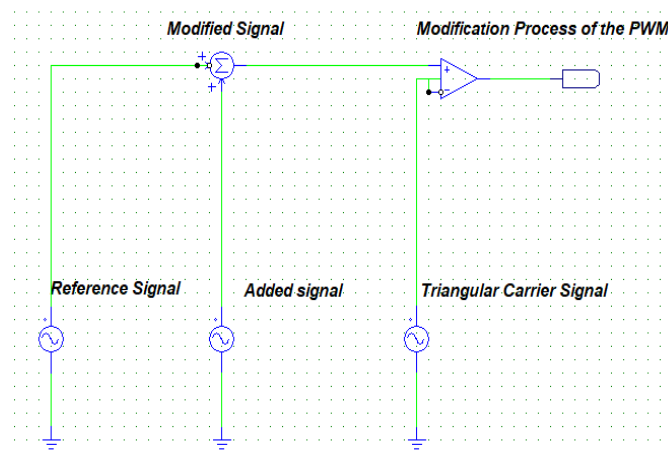


Figure 3. Modification process of the pulse width modulation

The reference signal was altered by integrating two signals. The primary reference and auxiliary signals are sine waveforms characterized by a fundamental frequency. In contrast, the supplementary signal has specifically defined values for its parameters. The reference signal was modified by combining two signals. The reference and auxiliary signals are sine waveforms specified by a fundamental frequency, whereas the supplementary signal possesses precisely defined waveform characteristics. Figure 4(a) illustrates a reference sine wave with a magnitude of 3, an average frequency of 50 Hz, and a phase shift of 0 degrees. Figure 4(b) and Figure 4(c) present both signals, which are combined to form a modified reference signal, subsequently compared with the triangular carrier waveform within the MPWM framework [26].

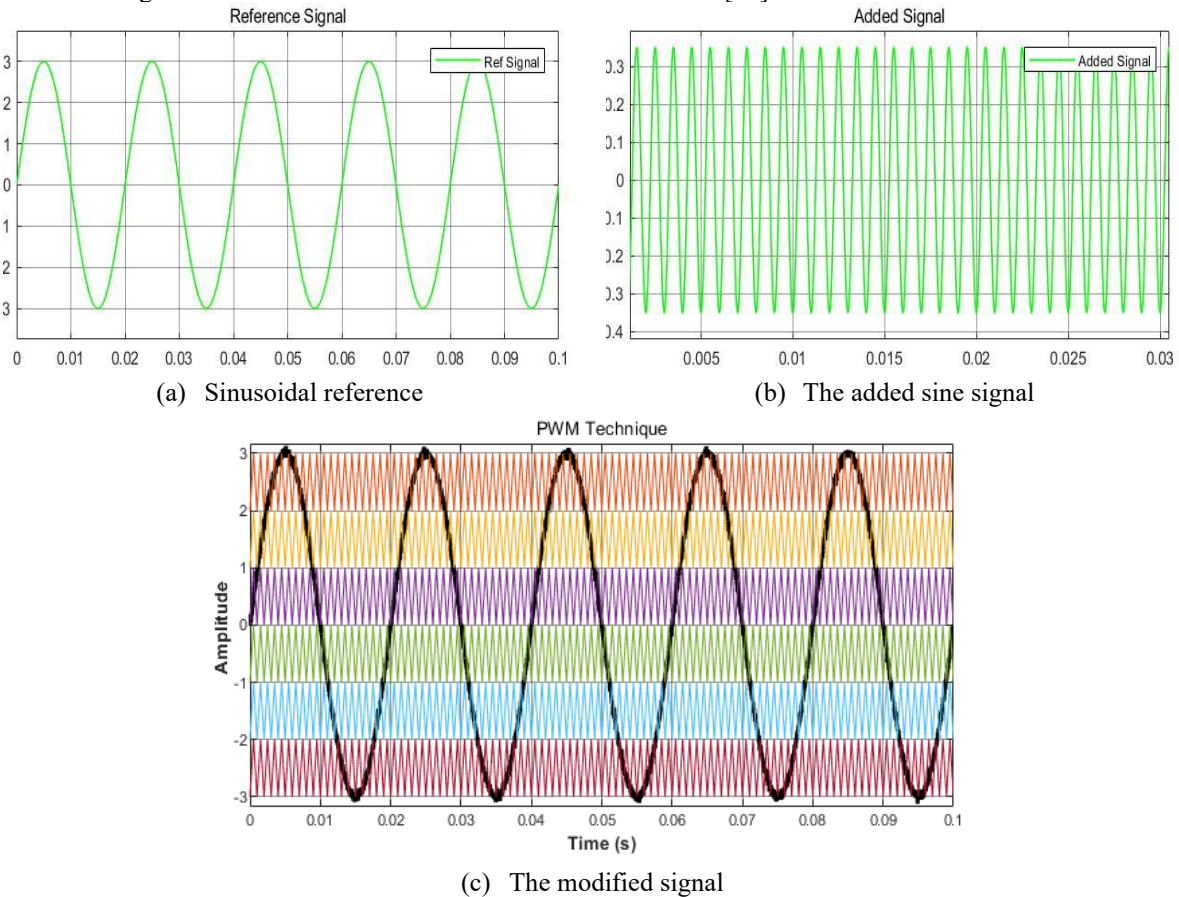


Figure 4. The process of generating an MPWM signal.

2.3 Particle Swarm Optimization

Metaheuristic-based optimization strategies are gaining popularity for addressing complicated real-world situations. The categorization of metaheuristic algorithms can be classified into three principal categories: evolutionary-based algorithms (e.g., GA, DE), swarm-based methodologies (e.g., PSO, GWO, WOA, SSA). The Particle Swarm Optimization method was developed by James Kennedy and Russell Eberhart in 1995. It functions as an effective method for addressing complex optimization problems, with the mobility and flocking behavior of avians forming the foundation for PSO [28]. The algorithm begins with the creation of a randomly generated population.

A genetic algorithm begins with the stochastic assignment of a population, representing the target solution set, which comprises chromosomes composed of a random combination of ones and zeros, or genes. Upon successful creation of the population, the subsequent phase entails a process termed "selection." During the selection process, the fitness function of each individual is evaluated, and the individual with the highest fitness function value is selected for further consideration. The Roulette wheel selection method is a renowned approach for choosing. Upon completion of the selection in the optimization process, the subsequent stage entails crossover. While numerous types of crossovers exist, single-point and two-point crossovers are the most common in mating among people. Typically, when a population experiences mutation, the goal is to maintain the population's diversity. A prevalent technique for executing mutation involves altering a gene's value to a randomly generated number within the $[0,1]$ interval, followed by the random selection of a threshold value. For any genes assigned values exceeding the threshold, we can either take the complement of their values or exchange them. The subsequent generation's population is derived from the population produced by executing all of these procedures. Generally, the new population comprises a greater number of fitter individuals than its predecessor.

Eventually, these procedures will be reiterated, though with reduced efficacy in enhancing the population. Particles denote the individual components of every swarm. In Particle Swarm optimization (PSO), each particle is assigned a position and a velocity, after which its fitness or objective function is assessed. In contrast to Genetic Algorithms, Particle Swarm optimization omits crossover and mutation processes, instead utilizing the exploitation of local optima for each particle and a global optimum for the entire population. The velocity and position of each particle are modified based on the best-known neighborhood of the individual's neighbors. This process continues until a solution is identified [29]. In this algorithm, each particle signifies a prospective solution and comprises two essential vectors: the position vector x , indicating its current location, and the velocity vector v , which delineates the trajectory the particle will follow in the absence of external forces. Every particle has connected with it a location vector and a velocity vector. As an example, each M^{th} iteration the current position vector associated with each i^{th} particle is shown by C_{i^m} and the velocity vector with which the particle is going to move is denoted by V_{i^m} . Particle i moves in the space according to its velocity V_{i^m} [30], [31]. At each iteration, particle positions are updated according to redefined velocity and position update rules given by Equation (8). At each cycle, the subsequent position is revised as Tone Eberhart, this population-based metaheuristic is a robust technique for addressing highly complex optimization problems. Without proper contextualization, however, the information can appear as disjointed fragments rather than cohesive supporting evidence. At each iteration, particle positions are updated according to predefined velocity and position update rules.

$$C_{i^{m+1}} = C_{i^m} + V_{i^{m+1}} \quad (8)$$

so that, where m denotes the current position and $m+1$ signifies the subsequent position. The velocity vector is modified as Equation (9).

$$V_{i^{m+1}} = w \cdot V_{i^m} + c_1 \cdot r_1 \cdot (P_{best} - C_{i^m}) + c_2 \cdot r_2 \cdot (G_{best} - C_{i^m}) \quad (9)$$

The random variables both r_1 and r_2 are restricted to the interval $[0, 1]$.

The Particle Swarm Optimization (PSO) algorithm was utilized to determine the optimal switching angles for minimizing the Total Harmonic Distortion (THD). The overall flow of the proposed PSO procedure is depicted in Figure 5, which systematically represents the initialization, fitness evaluation, velocity and position updating, and termination stages.

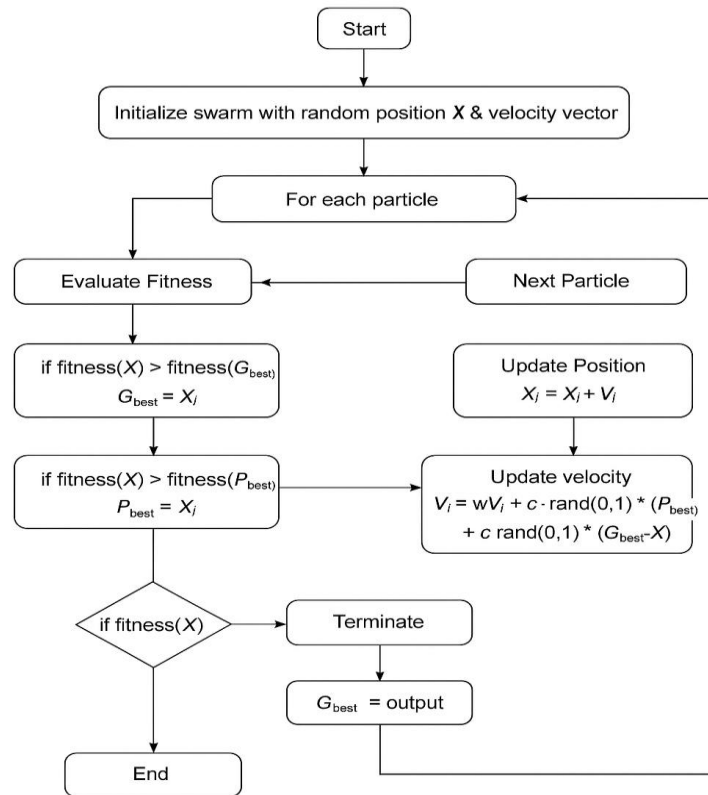


Figure 5. Flowchart of the Particle Swarm Optimization (PSO) algorithm

Algorithm 1 presents the Particle Swarm Optimization (PSO) procedure. The vector P_{best} corresponds to the position vector associated with the particle's best-known location, whereas G_{best} refers to the position vector corresponding to the best location identified by any particle in the swarm. The coefficients C_1 and C_2 act as acceleration factors [30].

Algorithm 1 Particle Swarm Optimization

```

1: Repeat until termination condition is satisfied
2: Initialize swarm with random  $C_0$  and  $V_0$ 
3: Initialize  $c_1$ ,  $c_2$ ,  $r_1$ ,  $r_2$ ,  $k$ ,  $kmax$ , and stop condition
4: while not termination condition do
5:   for each particle do
6:     Evaluate Fitness
7:     if  $fitness(X_i) > fitness(G_i)$  then
8:        $G_{best} \leftarrow C_i$ 
9:     end if
10:    if  $fitness(X_i) > fitness(P_i)$  then
11:       $P_{best} \leftarrow C_i$ 
12:    end if
13:  end for
14:  Update the particles velocity  $V_i^m$ 
15:  Update the particles position  $C_i^m$ 
16: end while
17: return  $G_{best}$ 

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A particle swarm optimization (PSO) framework was implemented with 50 particles and a maximum of 200 iterations. The inertia weight was linearly varied from 0.1 to 1.0, while both acceleration coefficients were fixed at 2.05 in accordance with Clerc's recommendation. Stable convergence was further supported through the application of a constriction factor of approximately 0.729. The search space for switching angles was restricted to $[0, 0.50]$, with the modulation index defined over 0–180 degrees. To prevent excessive oscillations, particle velocities were constrained to 10% of their respective variable ranges. Premature convergence was addressed by introducing a stagnation threshold of 100 iterations, combined with a partial reinitialization of 30% of the least-performing particles. Two asymmetric DC sources supplied the inverter under consideration, rated at 60 V and 20 V.

Algorithm 2 outlines the PSO fitness evaluation process, in which total harmonic distortion (THD) is adopted as the objective function with boundary constraints. The resulting global best solution represents the optimized switching angles that minimize harmonic distortion.

Algorithm 2 PSO-Based Switching Angle Optimization for THD Minimization

Require: Number of particles $nP = 50$; maximum iterations = 200; inertia weight $w \in [0.1, 1]$ (random at each iteration); $c_1 = 2.05$, $c_2 = 2.05$

Ensure: Optimized switching angles minimizing THD

```

1: Initialize the positions and velocities of  $nP$  particles (decision variables).
2: for each particle do
3:   Evaluate fitness (THD) and assign  $pbest$  and  $gbest$ .
4: end for
5: for  $iter = 1$  to maximum iterations do
6:   Randomly assign inertia weight  $w \in [0.1, 1]$ .
7:   for each particle do
8:     Update velocity:

$$v = wv + c_1 \text{rand}() (pbest - position) + c_2 \text{rand}() (gbest - position)$$

9:     Update position and apply boundary constraints.
10:    Re-evaluate fitness and update  $pbest$  and  $gbest$  if improved.
11:   end for
12: end for
13: return  $gbest$  (optimal switching angles).

```

As shown in Figure 6 the MATLAB/Simulink model of the proposed seven-level PUC inverter. The system utilizes IGBT switches featuring two DC-link voltages. A modulated PWM (MPWM) approach produces the initial switching signals, whereas a PSO algorithm delivers the optimal switching angles utilized in the gate drive circuit. This system generates a seven-level stepped output with less total harmonic distortion and enhanced power quality.

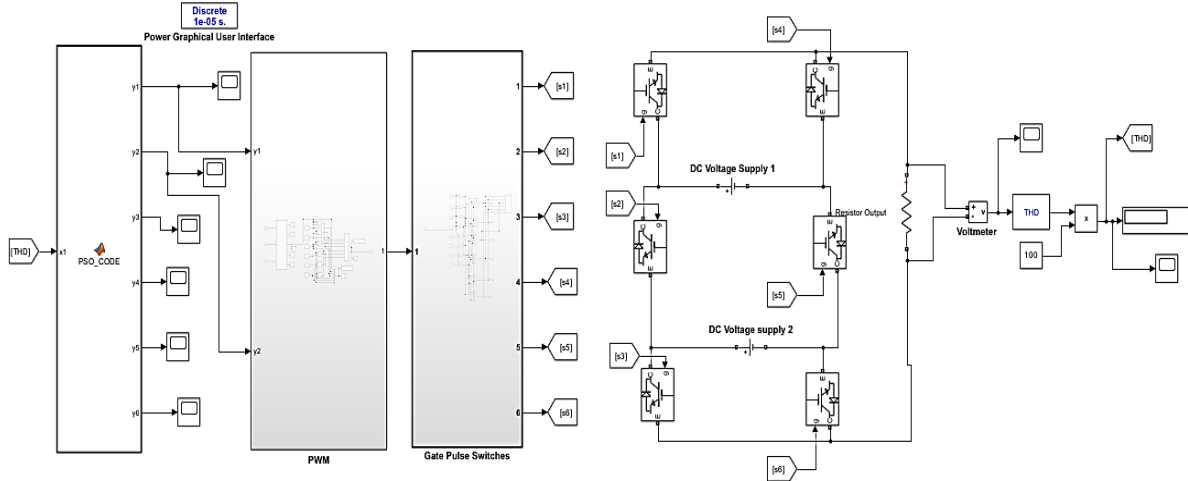


Figure 6. Simulink model of the seven-level Packed U-Cell (PUC)

According to the block structure illustrated in Figure 6, the proposed 7-level PUC inverter system was implemented in MATLAB/Simulink R2022a using the Simscape Electrical and Sim Power Systems block sets. The semiconductor devices were modeled using the IGBT/diode block from the Simscape library, which was parameterized to emulate typical commercial devices; no vendor-specific part numbers were applied. The inverter was powered by two disparate DC-link voltages of 60 V and 20 V, in accordance with the compact U-cell arrangement. A fixed-step discrete solver was adopted with a simulation sampling time of 1 μ s, ensuring high resolution for both transient and harmonic analysis. The inverter was connected to a pure resistive load of 10 Ω , which provided a straightforward test case for validating the output waveform quality. The gating signals were synthesized using a Modified Pulse Width Modulation (MPWM) block, in which a sinusoidal reference waveform was compared with multiple triangular carriers to generate the required switching pulses for the seven-level output. These signals were subsequently processed by a Gate Driver block, which introduced level shifting and dead-time insertion to ensure safe IGBT operation without cross-conduction. To guarantee reproducibility, a fixed random-seed policy was applied throughout the optimization process. Each case was simulated ten repeated runs, and averaged values of output voltage, current, and Total Harmonic Distortion (THD) were reported to minimize stochastic bias. Finally, custom MATLAB post-processing scripts were utilized to compute THD, extract harmonic spectra, and generate both time-domain and frequency-domain plots. These specifications fully define the experimental setup and enable replication of the reported results. The corresponding values are presented in Table 3.

Table 3. Simulation parameters for the 7-Level Packed U-Cell (PUC) inverter

| Parameter | Value/Setting |
|--------------------------|-----------------|
| DC-link voltages | 60 V and 20 V |
| Simulation sampling time | 1 μ s |
| Load type | R = 10 Ω |

3. RESULTS AND DISCUSSION

3.1 Performance of the Inverter Prior to Optimization

The performance evaluation of the inverter in the first instance revealed the absence of optimization for the switching conditions, from which a high level of harmonic distortion emerged. This challenge was resolved by optimizing the switching angles using Particle Swarm Optimization, or PSO.

The results of the PSO application offer remarkable enhancement for the harmonic performance of the 7-level PUC multilevel inverter. The initial Total Harmonic Distortion (THD) of 68.01% was reduced to 17.72% subsequent to the switching angles optimization by PSO. During this optimization, the dominant harmonics were aggressively suppressed, and the generated output waveform achieved close to a perfect sinusoidal waveform in accordance with the desired reference. The results of PSO confirm it as a robust approach for enhancing inverter performance and power quality proportional to the compliance with harmonic limitations, thus proving its feasibility for reliable practical use. This substantial reduction underscores the fundamental importance of optimization algorithms in the elimination of harmonics and emphasizes PSO as a viable option in contrast to traditional modulation techniques.

We developed an inverter model with Simulink, which was regulated with a distinctive PWM methodology, with the DC-link voltages V_{DC1} and V_{DC2} set to 60 V and 20 V, respectively. The output voltage's overall harmonic distortion was directly affected by the inverter's switching sequence. In the initial configuration,

the switching sequence was deliberately adjusted to produce a high THD level; therefore, we established an auxiliary signal with specific signal characteristics to enhance the optimization of the switching sequence and assess the THD. To meticulously regulate these parameters, we devised an PSO that generated random values within certain limits and computed the resultant THD of the aggregated signal. Candidate values for the parameters would have THD deleted if the newly computed value surpassed the previous optimum. Nevertheless, we would consider and present the most suitable alternatives if the harmonic were indeed lower. To avoid convergence to local optima and pursue the best solution in the entire search space, the operation was executed 100 times using default parameters. The algorithm achieved a minimum total spectral distortion value of 17.72%

3.2 Optimization Process and Convergence

The system produces a stepped voltage waveform at its output, and the multilevel inverter is analyzed to assess its capability in delivering a pure AC waveform appropriate for power conversion applications. By implementing the PWM technique, the inverter synthesizes a stepped voltage waveform that approximates a pure sinusoidal signal with reduced harmonic content, as depicted in Figure 7. The MPWM technique, combined with optimized switching angles, enhances the spectral quality of the output voltage, reducing unwanted harmonic components.

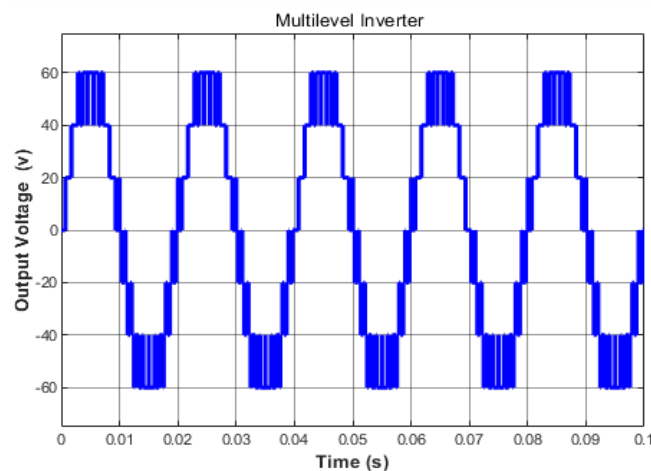


Figure 7. The 7-level Packed U-Cell (PUC) inverter output voltage

It was observed that PSO optimization algorithm achieved a high level of convergence between initial parameters ($A = 0.500$ V, $f = 1775.00$ Hz, 0.384419 rad) and the final optimal solution ($A = 0.143$ V, $f = 162$ Hz, 0.22 rad) as in Table 4. The optimized injection parameters obtained a 71.5 % percent amplitude reduction and 90.9 % percent frequency reduction, moving away the high-order harmonic targeting, and to strategic low-order harmonic cancellation. This convergence corresponds to improved algorithm efficiency and requires 92 percent less injection power, achieving a higher quality of THD reduction performance.

Table 4. PSO Injection Parameter Comparison

| Case | Frequency | Amplitude | Phase | THD |
|----------------------------|------------|-----------|--------------|-------|
| Before Optimized Injection | 1775.00 Hz | 0.500 V | 0.384419 rad | 68.01 |
| After Optimized Injection | 162 Hz | 0.143 V | 0.22 rad | 17.72 |

As illustrated in Figure 8 the PSO convergence behavior for THD minimization in a seven-level multilevel inverter. The results show that the injection amplitude stabilizes at 0.143 V, the frequency converges rapidly to 162 Hz, and the phase settles around 2.2 rad (126°) after an initial steep adjustment. These trajectories highlight the distinct roles of each parameter: amplitude ensures balanced modulation strength, frequency shapes harmonic interaction, and phase alignment proves especially critical for cancellation effectiveness. The observed convergence underscores PSO's efficiency in navigating the nonlinear and multimodal landscape of inverter optimization. By balancing exploration and exploitation, the algorithm avoids local minima and consistently identifies globally effective parameter sets. This demonstrates the suitability of swarm intelligence methods for advanced power electronics applications, where precise parameter tuning directly translates to improved harmonic performance and reduced THD.

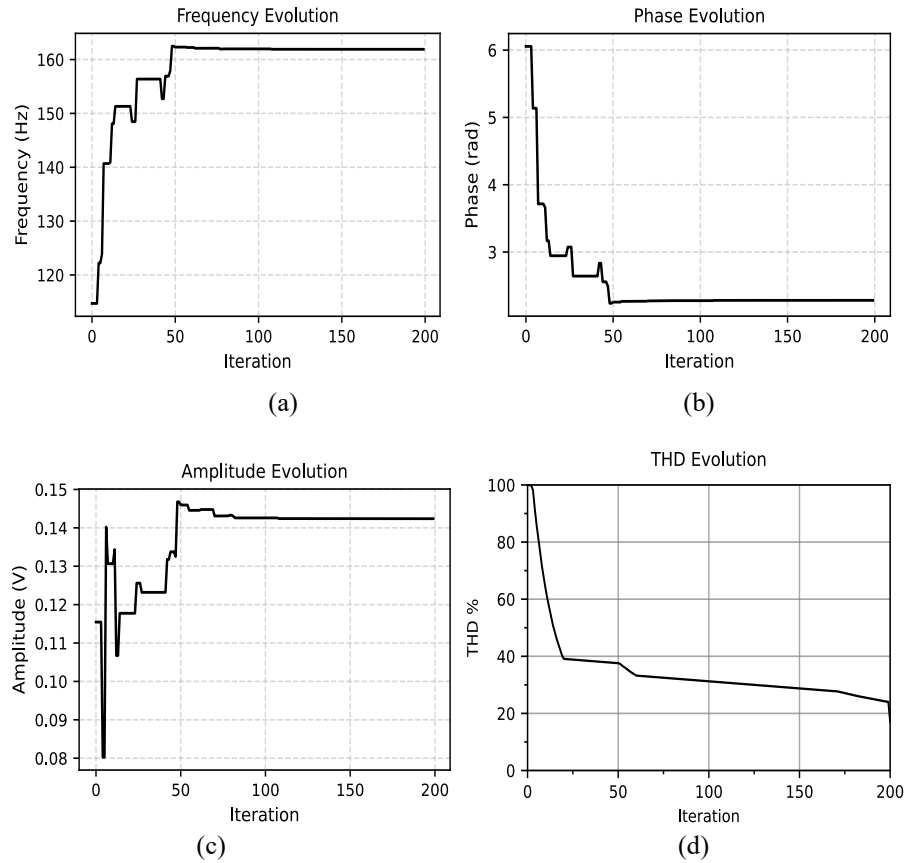


Figure 8. Simulation results of the optimized injected signal

The varying rates of convergence among the three parameters illustrate that the specific sensitivities inherent in the target objective function are the frequency interpolates, which converge rapidly, as minor deviations significantly impact the generated harmonic envelope. In contrast, amplitude and phase display slower convergence due to their interdependence and the nuanced manner in which they influence harmonic cancellation. To mitigate the risk of emergent patterns becoming excessively focused too early, the foundational evolutionary strategy meticulously regulates diversity, enabling populations to progress towards the parameter basin of attraction while effectively suppressing premature convergence gradients. The outcome is a resilient global minimum, as evidenced by the consistent, low variance estimates at the conclusion of the run: amplitude 0.143 V, frequency 162 Hz, and phase 2.2 rad, all documented without indications of overshoot, residual oscillation, or other artifacts of adaptation-induced instability.

3.3 Harmonic Spectrum Analysis and Power Quality Improvement

Figure 9 presents the output waveforms and harmonic spectra of the 7-level PUC multilevel inverter at selected amplitude modulation indices ($m = 0.2, 0.3, 0.4$, and 0.5). These cases demonstrate the dependence of harmonic performance on the modulation index when switching angles are optimized using the PSO algorithm. The inverter achieves its optimum performance at $m = 0.1$, where the optimized switching angles minimize the total harmonic distortion (THD) to 17.72%. As the modulation index increases, THD rises monotonically, reflecting a systematic degradation in waveform quality. Although the figure illustrates cases up to $m = 0.5$ for clarity, the optimization was extended to $m = 1.0$, where the maximum distortion level was observed. This trend is consistent with the theoretical behavior of multilevel inverters, in which higher modulation indices redistribute harmonic components and complicate the suppression of distortion.

These results validate the effectiveness of the proposed PSO-based optimization method in minimizing THD. Emphasis on the best-case performance at $m = 0.1$ underscores the capability of the approach to significantly improve the harmonic profile and enhance the overall output quality of the inverter.

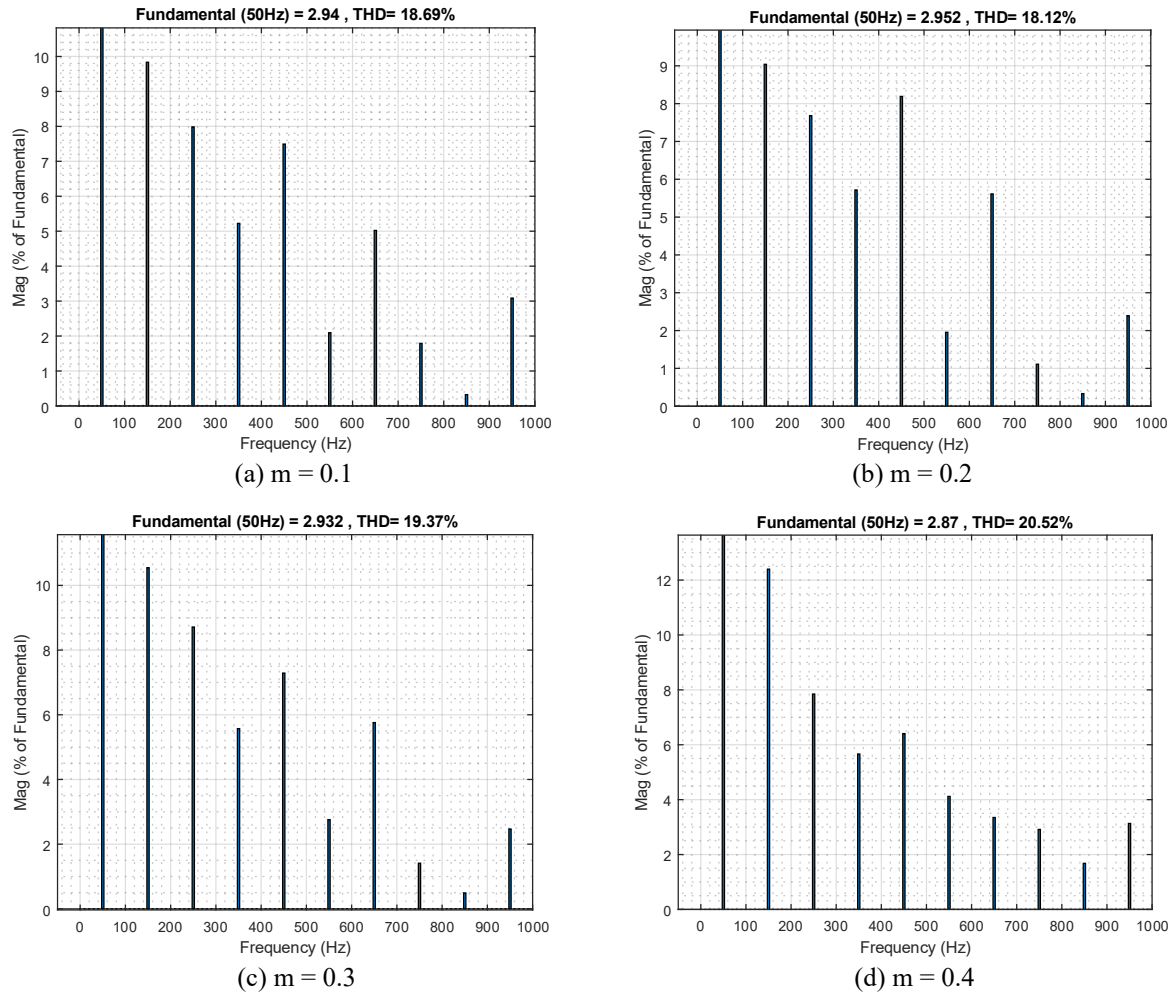


Figure 9. Harmonic spectra at different amplitude modulation indices.

It can be seen from Figure 10 that a conducted to evaluate the inverter's performance by examining the harmonic spectrum, as seen in Figure 9. The research reveals that the total harmonic distortion (THD) of the output voltage decreases from 68.01% to 17.72% when the Particle Swarm Optimization method modifies the switching angles. The enhancement in THD confirms the efficacy of the MPWM method and PSO-based optimization in augmenting the inverter's power quality. Optimizing switching angles effectively suppresses lower-order harmonics, hence enhancing system efficiency and reducing power losses. The findings validate that the amalgamation of computational intelligence approaches with sophisticated modulation methods can significantly improve the efficacy of multilevel inverters across diverse industrial and renewable energy applications.

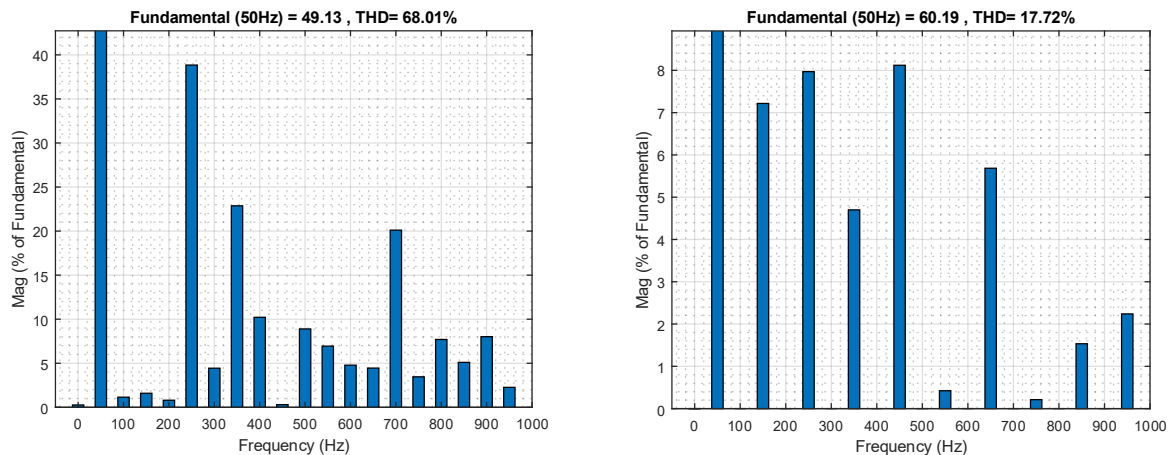


Figure 10. Spectral analysis of harmonics

3.4 Comparative Analysis with Prior Literature

The PSO-based optimization significantly reduces harmonics by dynamically adjusting switching angles and preventing premature convergence to local minima. This method illustrates the balance between exploration and exploitation, which is essential to metaheuristic optimization. In Ref. [12] noted comparable results, demonstrating that the hybrid GA–PSO consistently outperformed individual algorithms due to enhanced solution diversity and expedited local convergence. It has been demonstrated that the implementation of PSO-optimized SHE-PWM in cascaded H-bridge inverters markedly reduces harmonics across all voltage levels, highlighting the critical role of fitness function design in effectively controlling both total harmonic distortion (THD) and specific harmonic orders [13]. In ref. [5], the effectiveness of population-based methods was further validated, demonstrating that the Wild Horse Optimization algorithm achieved competitive THD performance for PUC inverters, albeit with increased sensitivity to hyperparameter tuning.

Despite widespread consensus, many inconsistencies emerge when juxtaposing these findings across other investigations. Discrepancies in reported findings stem from variations in inverter architecture (PUC versus cascaded H-bridge), DC-link configuration (symmetric versus asymmetric sources), and objective functions (pure THD minimization versus weighted harmonic penalties). Furthermore, algorithmic hyperparameters such as swarm size, mutation rates, maximum iterations, and assessment methods (single-run versus repeated statistical runs, existence of output filters, and correctness of device models) substantially affect convergence behavior. The increased sensitivity reported in Ref. [5] is attributed to the diminished sample size and a stronger dependence on the initial population distribution, whereas the more consistent performance observed in this study reflects sustained convergence across multiple trials. The research demonstrates that population-based optimizers are reliable frameworks for minimizing THD, with discrepancies among studies primarily due to methodological differences rather than intrinsic factors.

A comparative evaluation with existing optimization-based multilevel inverter studies demonstrates that the proposed 7-level PSO-MPWM inverter achieves competitive performance with a THD of 17.72%. Research on asymmetric multilevel inverters using PSO optimization shows that a 7-level configuration achieves a THD of 15 level is 4.23%, while an 11-level system attains 11.17% [32]. Additionally, an ANFIS-PSO optimized cascaded multilevel inverter demonstrates THD values ranging from 10% to 8% depending on the modulation index and switching angles [33]. Recent investigations on PUC inverters using hybrid optimization algorithms [27], [12] have shown promising results in harmonic mitigation. The proposed 7-level system achieves comparable harmonic performance with a simplified topology, demonstrating an optimal trade-off between system complexity and harmonic suppression capability.

4. CONCLUSION

The findings validated that Particle Swarm Optimization (PSO) significantly diminished harmonic distortion in a 7-level Packed U-Cell (PUC) multilevel inverter, reducing THD from 68.01% without optimization to 17.72% with PSO, consequently demonstrating a significant improvement in output waveform quality. The convergence behavior demonstrated steady tuning of amplitude, frequency, and phase at globally optimal values, emphasizing the method's efficacy in tackling nonlinear, multimodal optimization problems. Comparative analysis revealed that the proposed PSO-MPWM inverter achieves competitive performance compared to other optimization-based designs, demonstrating an optimal trade-off between system complexity and harmonic suppression. Furthermore, prior studies on higher-level inverters reported slightly lower THD values, confirming that the presented 7-level topology offers a simplified yet efficient approach for harmonic reduction. This study enhances inverter control by demonstrating the innovative application of swarm intelligence for effective and flexible harmonic reduction, with hardware validation recognized as the subsequent essential phase.

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REFERENCE

- [1] K. Muralikumar and P. Ponnambalam, "Analysis of cascaded multilevel inverter with a reduced number of switches for reduction of total harmonic distortion," *IETE Journal of Research*, vol. 69, no. 1, pp. 295–308, Jan. 2023. <https://dx.doi.org/10.1080/03772063.2020.1819450>

- [2] Y. Babkrani, G. Mourad, A. Naddami, K. Choukri, and S. H. Mounir, "Implementation of a modified carrier-based PWM technique for a cascaded MLI using DSP microcontroller," *Int. J. Power Electron. Drive Syst.*, vol. 14, no. 3, pp. 1523–1533, Sep. 2023. <https://dx.doi.org/10.11591/ijpeds.v14.i3.pp1523-1533>
- [3] M. Trabelsi, A. N. Alquennah, and H. Vahedi, "Review on single-DC-source multilevel inverters: Voltage balancing and control techniques," *IEEE Open J. Ind. Electron. Soc.*, vol. 3, pp. 711–732, 2022. <https://dx.doi.org/10.1109/OJIES.2022.3221015>
- [4] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002. <https://dx.doi.org/10.1109/TIE.2002.801052>
- [5] A. Balal, S. Dinkhah, F. Shahabi, M. Herrera, and Y. L. Chuang, "A review on multilevel inverter topologies," *Emerging Science Journal*, vol. 6, no. 1, pp. 185–200, Feb. 2022. <https://dx.doi.org/10.28991/ESJ-2022-06-01-014>
- [6] F. Ebrahimi, N. A. Windarko, and A. I. Gunawan, "Wild horse optimization algorithm implementation in 7-level packed U-cell multilevel inverter to mitigate total harmonic distortion," *Electr. Eng. Electromech.*, vol. 2024, no. 5, pp. 34–40, Aug. 2024. <https://dx.doi.org/10.20998/2074-272X.2024.5.05>
- [7] H. Vahedi, M. Sharifzadeh, and K. Al-Haddad, "Modified seven-level pack U-cell inverter for photovoltaic applications," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 3, pp. 1508–1516, Sep. 2018. <https://dx.doi.org/10.1109/JESTPE.2018.2821663>
- [8] A. Ben Zid, A. Lamari, and F. Bacha, "Seven-level grid-connected packed U-cells inverter using photovoltaic generators system," *Proc. Inst. Mech. Eng., Part I: J. Syst. Control Eng.*, vol. 237, no. 4, pp. 684–703, Apr. 2023. <https://dx.doi.org/10.1177/0959651820987955>
- [9] U. Krishnamoorthy, U. Pitchaikani, E. Rusu, and H. H. Fayek, "Performance analysis of harmonic-reduced modified PUC multi-level inverter based on an MPC algorithm," *Inventions*, vol. 8, no. 4, Aug. 2023. <https://dx.doi.org/10.3390/inventions8040090>
- [10] S. Y. Nikouei, B. M. Dehkordi, and M. Niroomand, "A genetic-based hybrid algorithm harmonic minimization method for cascaded multilevel inverters with ANFIS implementation," *Math. Probl. Eng.*, vol. 2021, 2021. <https://dx.doi.org/10.1155/2021/6642317>
- [11] H. Iqbal and A. Sarwat, "Improved genetic algorithm-based harmonic mitigation control of an asymmetrical dual-source 13-level switched-capacitor multilevel inverter," *Energies*, vol. 18, no. 1, Jan. 2025. <https://dx.doi.org/10.3390/en18010035>
- [12] B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "Harmonic optimization of multilevel converters using genetic algorithms," *IEEE Power Electron. Lett.*, vol. 3, no. 3, pp. 92–95, Sep. 2005. <https://dx.doi.org/10.1109/LPEL.2005.856713>
- [13] H. Iqbal and A. Sarwat, "Design and implementation of hybrid GA-PSO-based harmonic mitigation technique for modified packed U-cell inverters," *Energies*, vol. 18, no. 1, Jan. 2025. <https://dx.doi.org/10.3390/en18010124>
- [14] M. Sadoughi, A. Pourdashnia, M. Farhadi-Kangarlu, and S. Galvani, "PSO-optimized SHE-PWM technique in a cascaded H-bridge multilevel inverter for variable output voltage applications," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8065–8075, Jul. 2022. <https://dx.doi.org/10.1109/TPEL.2022.3146825>
- [15] M. N. Hamidi and D. Ishak, "Particle swarm optimization effectiveness for selective harmonic elimination in multilevel inverters at varying output levels," *Majlesi J. Electr. Eng.*, vol. 19, no. 2, Jun. 2025. <https://dx.doi.org/10.57647/j.mjee.2025.1902.38>
- [16] F. A. Izzaqi, N. A. Windarko, and O. A. Qudsi, "Minimization of total harmonic distortion in neutral point clamped multilevel inverter using grey wolf optimizer," *Int. J. Power Electron. Drive Syst.*, vol. 13, no. 3, pp. 1486–1497, Sep. 2022. <https://dx.doi.org/10.11591/ijpeds.v13.i3.pp1486-1497>
- [17] H. Vahedi and K. Al-Haddad, "Real-time implementation of a seven-level packed U-cell inverter with a low-switching-frequency voltage regulator," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5967–5973, Aug. 2016. <https://dx.doi.org/10.1109/TPEL.2015.2490221>
- [18] M. J. Mnati, A. H. Ali, D. V. Bozalakov, S. Al-Yousif, and A. Van den Bossche, "Design and implementation of a gate driver circuit for three-phase grid tie photovoltaic inverter application," in *Proc. 7th Int. Conf. Renew. Energy Res. Appl. (ICRERA)*, Oct. 2018, pp. 701–706. <https://dx.doi.org/10.1109/ICRERA.2018.8566923>
- [19] A. Azeem, M. K. Ansari, M. Tariq, A. Sarwar, and I. Ashraf, "Design and modeling of solar photovoltaic system using seven-level packed U-cell (PUC) multilevel inverter and zeta converter for off-grid application in India," *Electrica*, vol. 19, no. 2, pp. 101–112, 2019. <https://dx.doi.org/10.26650/electrica.2019.18053>

- [20] F. Ait Bellah, A. Abouloifa, S. Echalih, Z. Hekss, K. Naftahi, and I. Lachkar, "Control design of a seven-level packed U cell inverter," *IFAC-PapersOnLine*, vol. 55, no. 12, pp. 677–682, Jan. 2022. <https://dx.doi.org/10.1016/j.ifacol.2022.07.390>
- [21] M. Tariq et al., "Evaluation of level-shifted and phase-shifted PWM schemes for seven level single-phase packed U cell inverter," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 3, pp. 232–242, Sep. 2018. <https://dx.doi.org/10.24295/CPSSSTPEA.2018.00023>
- [22] I. A. Harbi, H. Z. Azazi, A. E. Lashine, and A. E. Elsabbe, "A higher levels multilevel inverter with reduced number of switches," *Int. J. Electron.*, vol. 105, no. 8, pp. 1286–1299, Aug. 2018. <https://dx.doi.org/10.1080/00207217.2018.1440429>
- [23] K. Ananthi and S. Manoharan, "Enhancing power quality using packed U cell 5 multilevel inverter-based shunt active power filter with fuzzy controller," *Int. J. Fuzzy Syst.*, vol. 24, no. 3, pp. 1356–1370, Apr. 2022. <https://dx.doi.org/10.1007/s40815-021-01194-8>
- [24] N. Mishra et al., "Performance assessment of eight-switch 11-level packed U cell converter under dynamic solar photovoltaic environment," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 4, pp. 3851–3860, Aug. 2022. <https://dx.doi.org/10.1109/JESTPE.2021.3098828>
- [25] F. AbolqasemiKharanaq, A. Poorfakhraei, A. Emadi, and B. Bilgin, "An improved carrier-based PWM strategy with reduced common-mode voltage for a three-level NPC inverter," *Electronics*, vol. 12, no. 5, p. 1072, Feb. 2023. <https://dx.doi.org/10.3390/electronics12051072>
- [26] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002. <https://dx.doi.org/10.1109/TIE.2002.801073>
- [27] Z. Sifat et al., "Selective harmonic elimination in PUC-5 multilevel inverter using hybrid IGWO-DE algorithm," *Eng. Rep.*, vol. 6, no. 10, Oct. 2024. <https://dx.doi.org/10.1002/eng2.12883>
- [28] S. P. Lim and H. Haron, "Performance comparison of genetic algorithm, differential evolution and particle swarm optimization towards benchmark functions," in *Proc. IEEE Conf. Open Syst. (ICOS)*, 2013, pp. 41–46. <https://dx.doi.org/10.1109/ICOS.2013.6735045>
- [29] A. G. Gad, "Particle swarm optimization algorithm and its applications: A systematic review," *Arch. Comput. Methods Eng.*, vol. 29, no. 5, pp. 2531–2561, Aug. 2022. <https://dx.doi.org/10.1007/s11831-021-09694-4>
- [30] M. Joshi, M. Gyanchandani, and D. R. Wadhvani, "Analysis of genetic algorithm, particle swarm optimization and simulated annealing on benchmark functions," in *Proc. 5th Int. Conf. Comput. Methodol. Commun. (ICCMC)*, Apr. 2021, pp. 1152–1157. <https://dx.doi.org/10.1109/ICCMC51019.2021.9418458>
- [31] K. Y. Gómez Díaz, S. E. de León Aldaco, J. Aguayo Alquicira, and L. G. Vela Valdés, "THD minimization in a seven-level multilevel inverter using the TLBO algorithm," *Eng.*, vol. 4, no. 3, pp. 1761–1786, Sep. 2023. <https://dx.doi.org/10.3390/eng4030100>
- [32] D. Gireesh Kumar et al., "Design of an optimized asymmetric multilevel inverter with reduced components using Newton-Raphson method and particle swarm optimization," *Math. Probl. Eng.*, vol. 2023, no. 1, Jan. 2023. <https://dx.doi.org/10.1155/2023/9966708>
- [33] O. Sánchez Vargas et al., "ANFIS-PSO-based optimization for THD reduction in cascaded multilevel inverter UPS systems," *Electronics*, vol. 13, no. 22, p. 4456, Nov. 2024. <https://dx.doi.org/10.3390/electronics13224456>